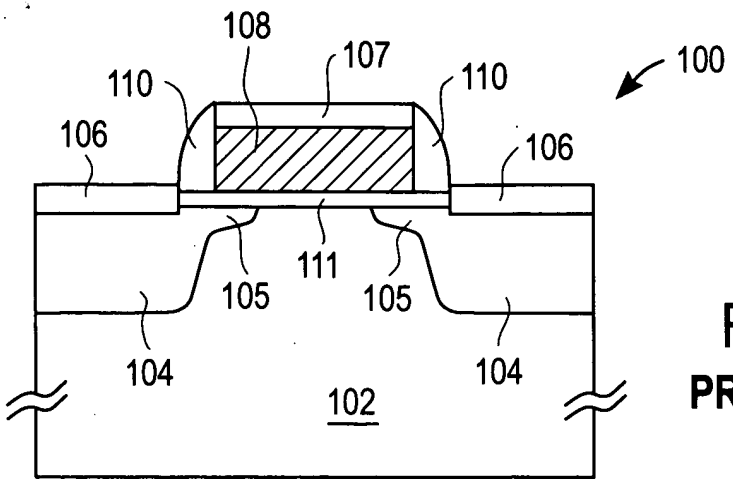


FIG. 1
PRIOR ART

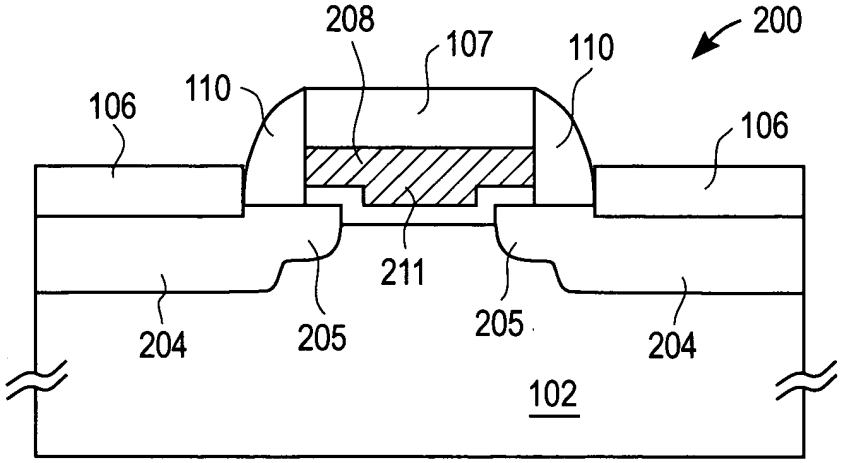


FIG. 2

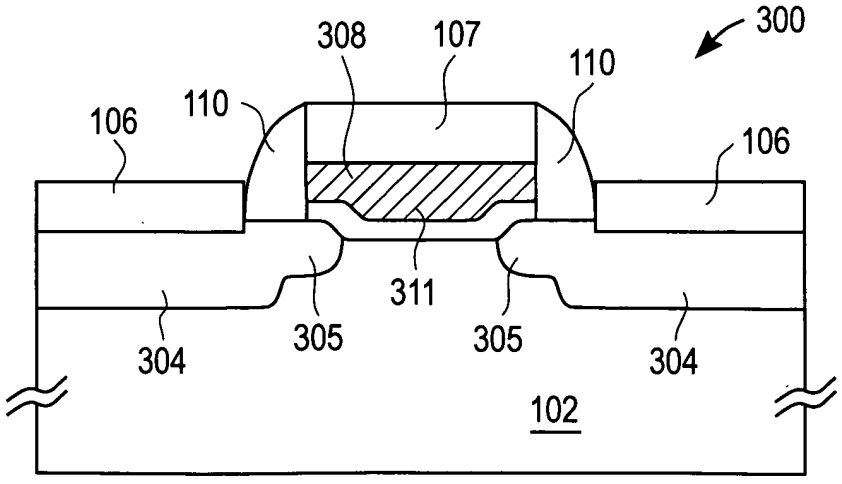


FIG. 3

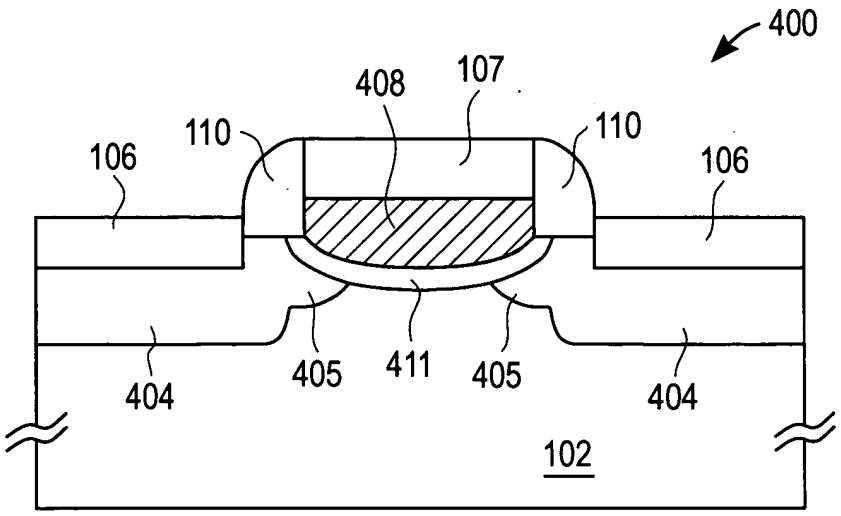


FIG. 4

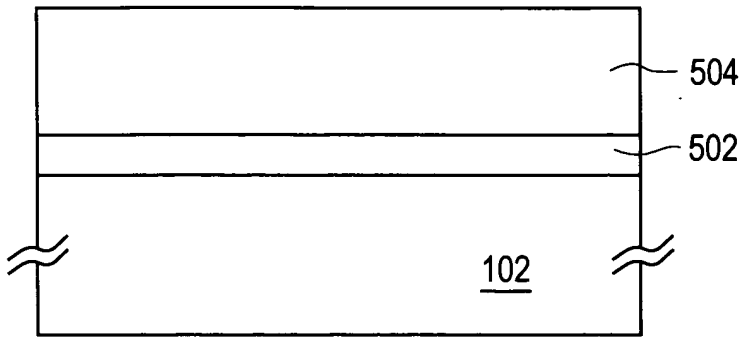
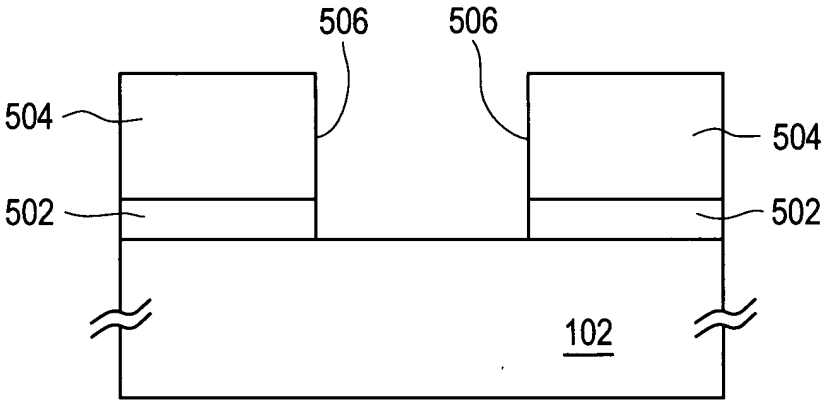


FIG. 5



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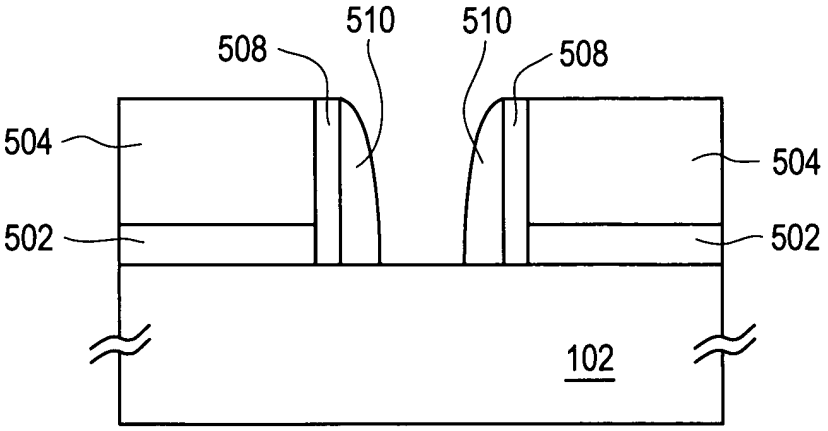

FIG. 7

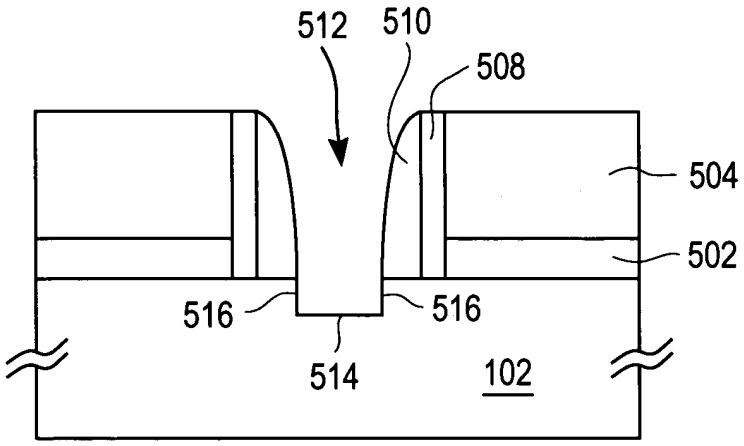

FIG. 8

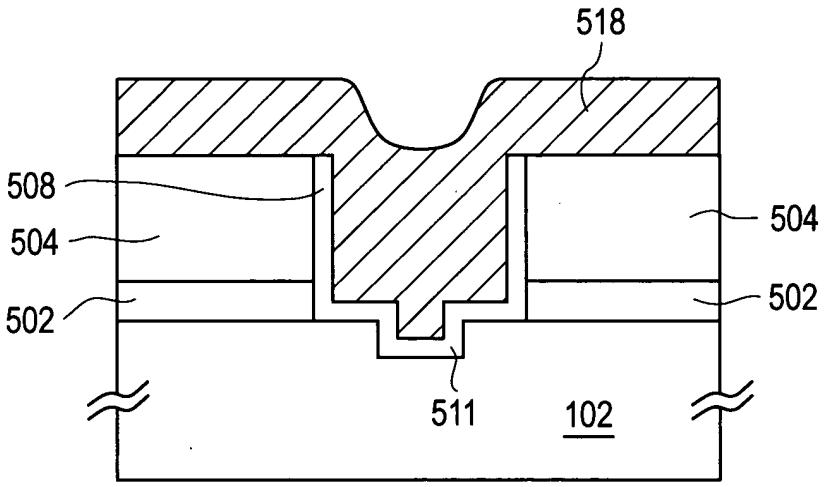

FIG. 9

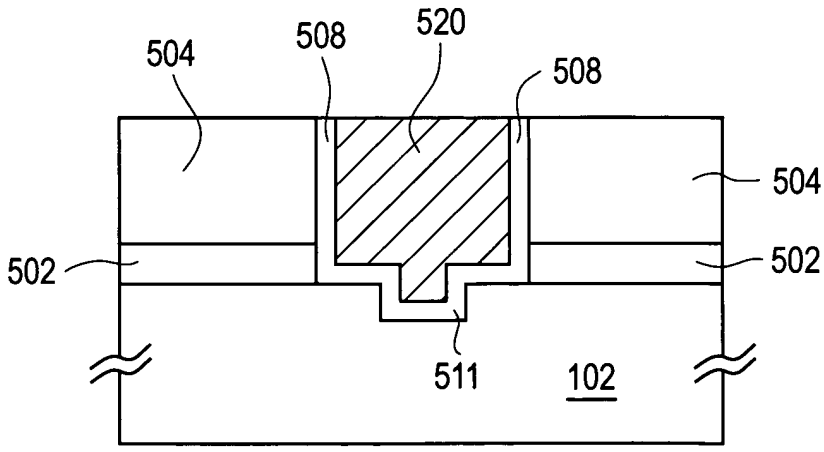

FIG. 10

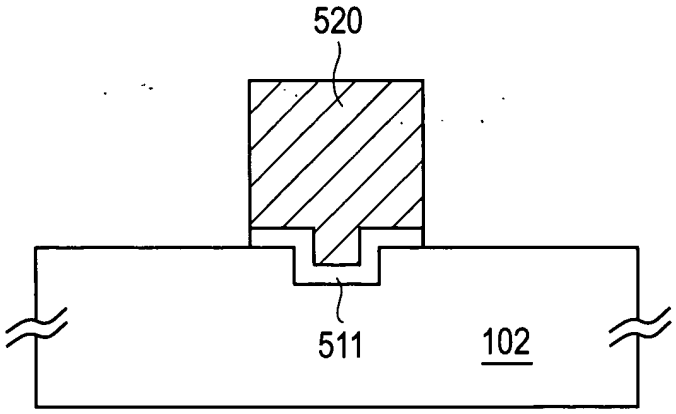

FIG. 11

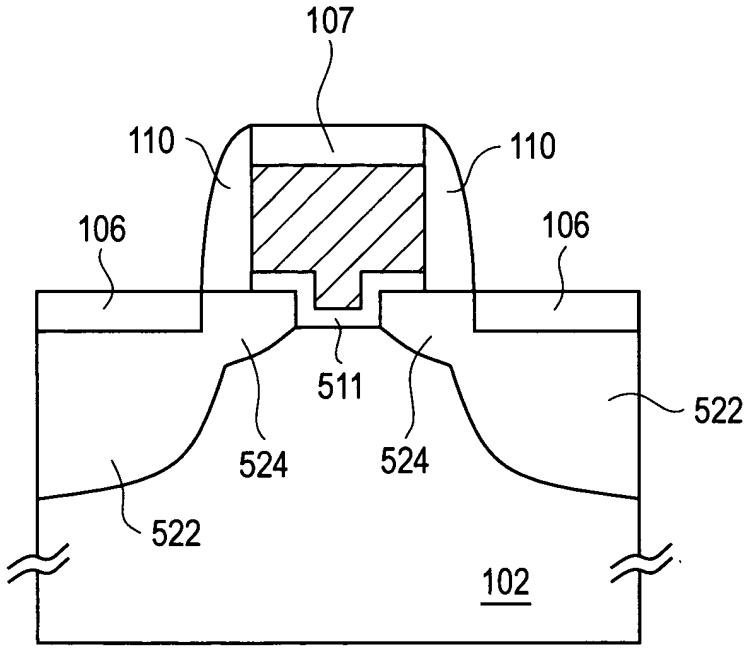

FIG. 12

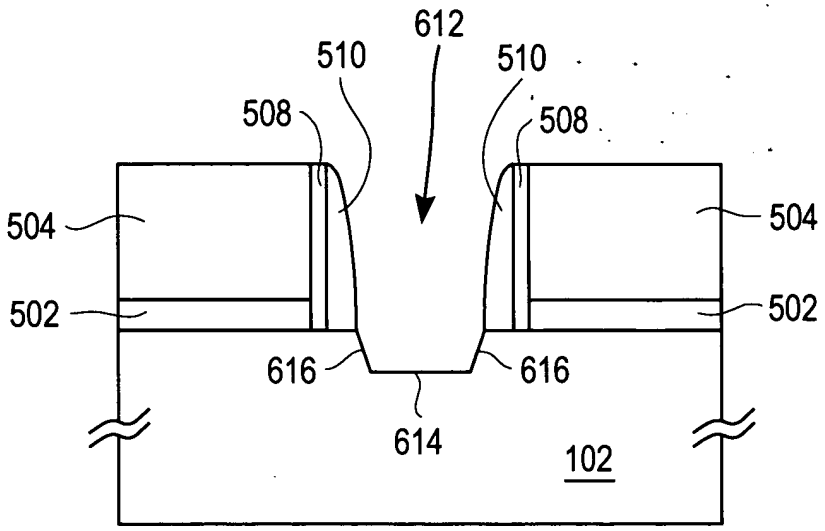
612
510
510
508
508
504
504
502
502
616
616
614
102

FIG. 13

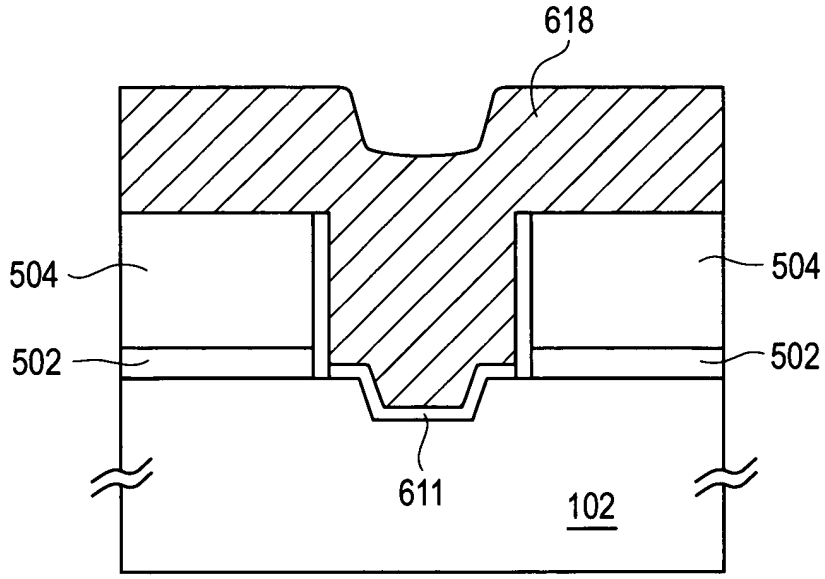
618
504
504
502
502
611
102

FIG. 14

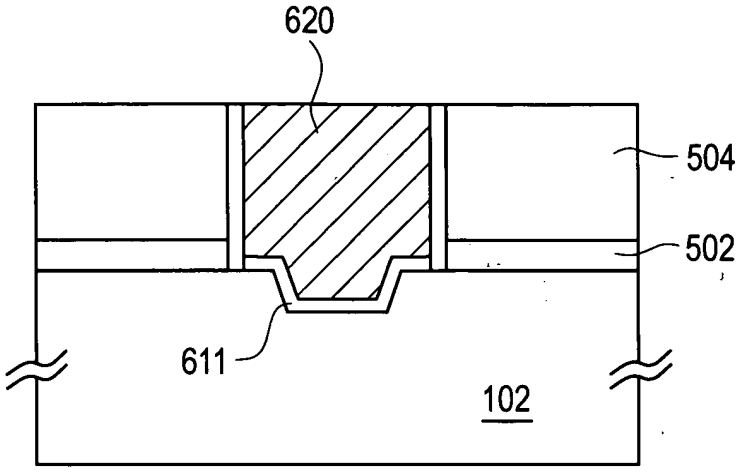

FIG. 15

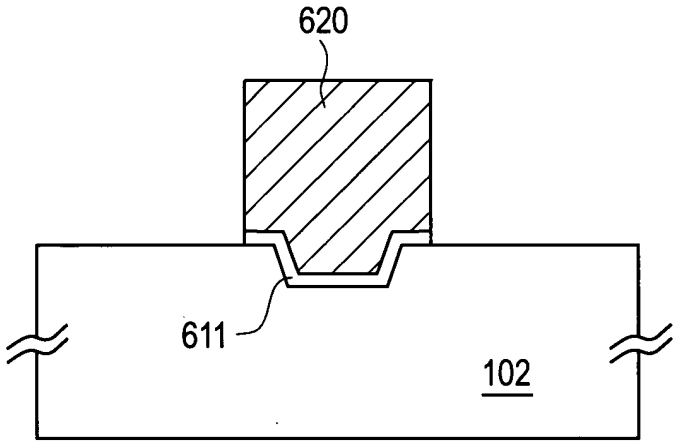

FIG. 16

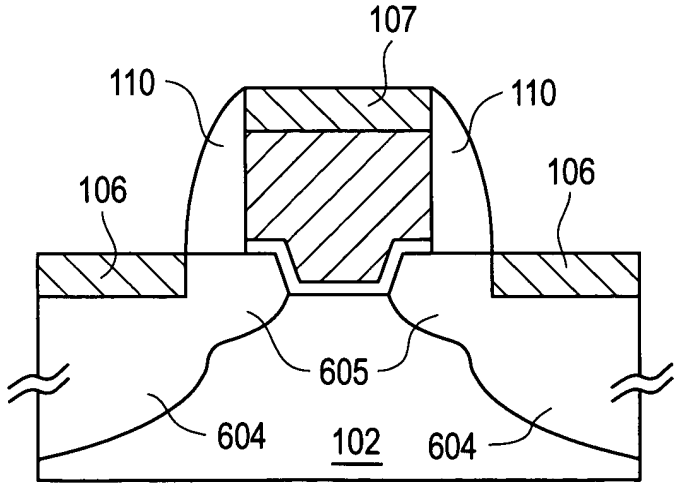

FIG. 17

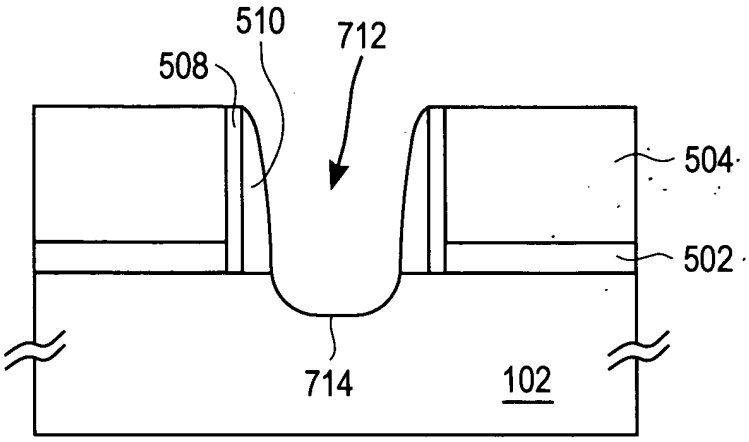

FIG. 18

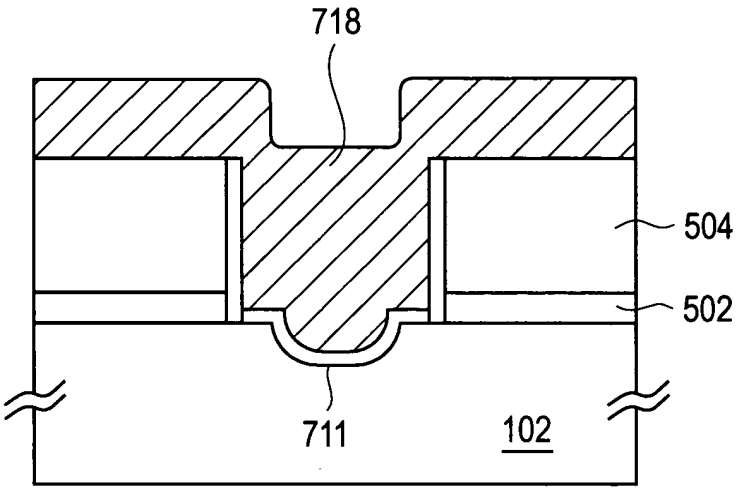

FIG. 19

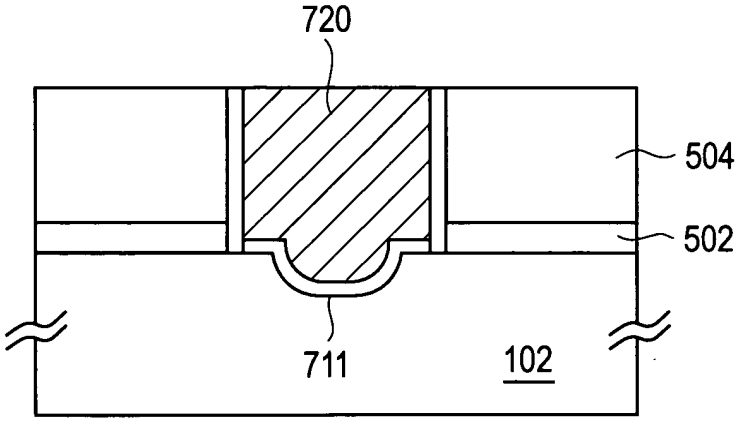

FIG. 20

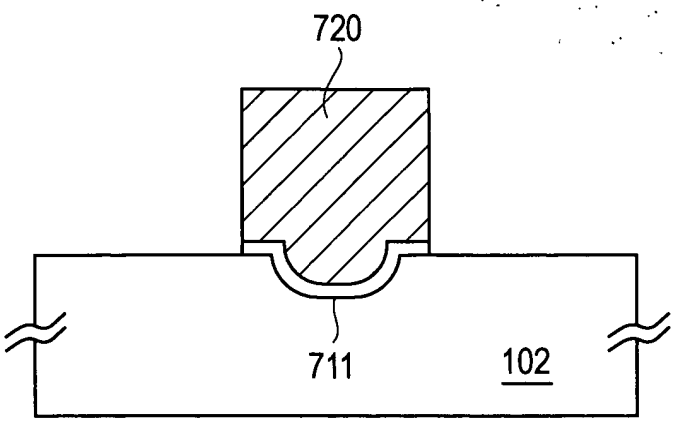

FIG. 21

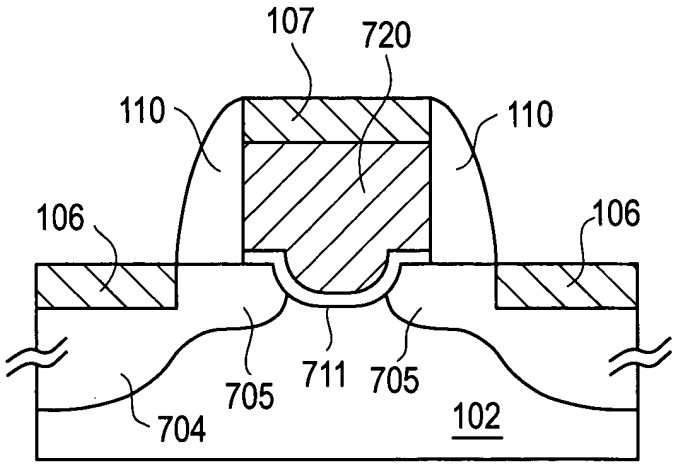

FIG. 22

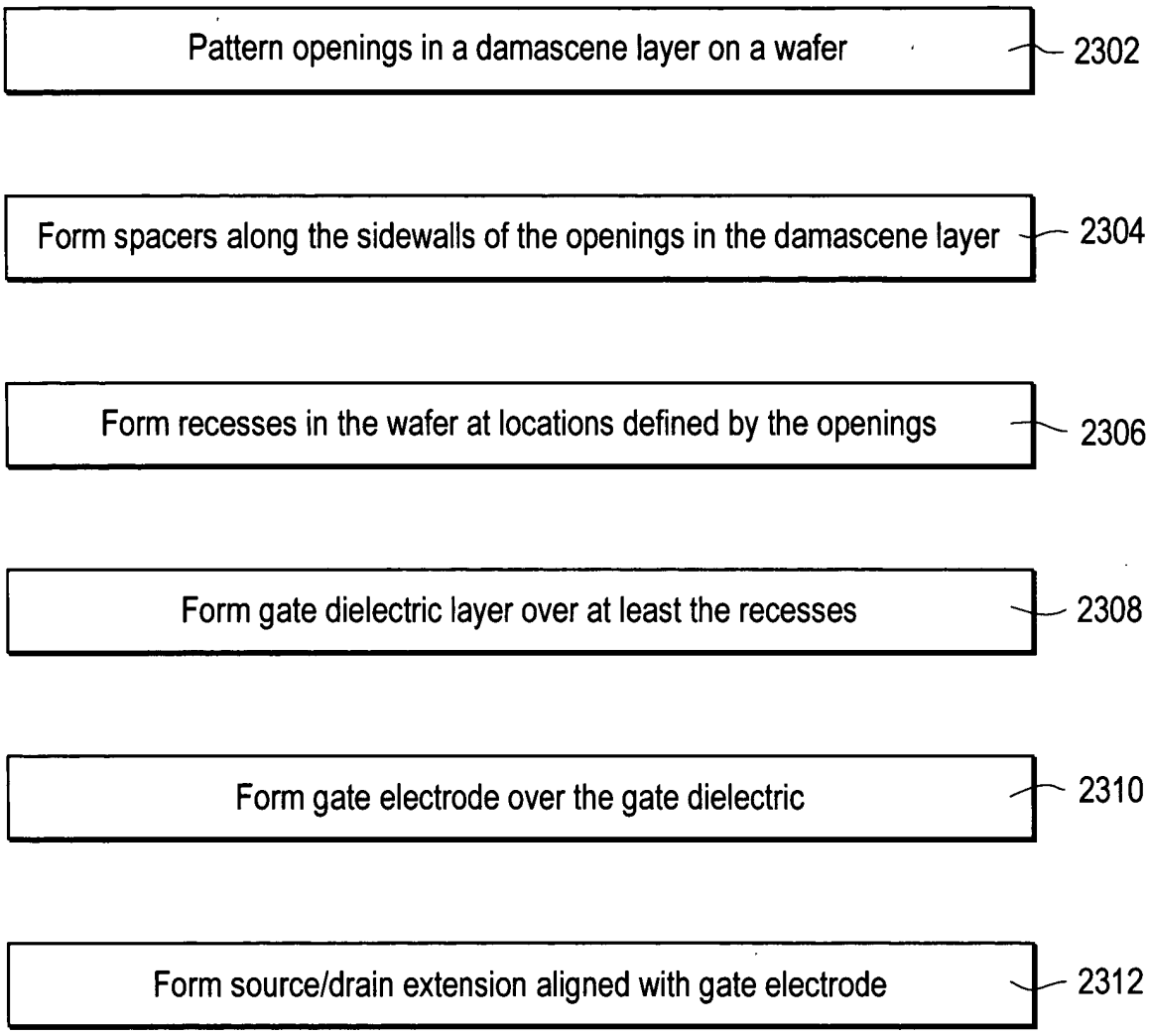
Pattern openings in a damascene layer on a wafer
2302
Form spacers along the sidewalls of the openings in the damascene layer
2304
Form recesses in the wafer at locations defined by the openings
2306
Form gate dielectric layer over at least the recesses
2308
Form gate electrode over the gate dielectric
2310
Form source/drain extension aligned with gate electrode
2312

FIG. 23